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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,986	09/12/2003	Louis K. Scheffer	CA7016672001	6083

23639 7590 04/17/2006

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,986	SCHEFFER, LOUIS K.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,7,12,13,17,18,23,24,28,29 and 34-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7,12,13,17,18,23,24,28,29 and 34-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/660,986 and RCE with amendment filed on 3/2/2006. Claims 1-2, 6-7, 12-13, 17-18, 23-24, 28-29 and 34-60 remain pending in the application.

Claim Objections

2. Claims 1, 12 and 23 are objected to because of the following informalities: phases "where it is possible to" and "can be made" are not accurate claim language. Phrase "avoiding pipelining" needed clarification, Examiner found no explanation as to it means. How the pipelining can be avoided when clocked element(s) are inserted or a number of clocked element is modified. Appropriate correction is required in order to avoid claimed construction problem.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-2, 6-7, 12-13, 17-18, 23-24, 28-29 and 34-60 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention appears to be an abstract idea rather than a practical application of idea because the claimed invention does not provide a useful, concrete and tangible result.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1, 6-7, 12, 17-18, 23, 28-29 and 34-60 are rejected under 35 U.S.C. 102(a) as being anticipated by Chow et al., "EVE: A CAD Tool for Manual Placement and Pipelining Assistance of FPGA Circuits," ACM, Feb. 2002, pp. 85-94.

6. As to claims 1, 12 and 23, Chow et al. teach a manual editor, called EVE, which can assist a designer to perform manual packing, placement and pipelining of an integrated circuit design to achieve a meaningful increase in performance (See abstract and whole document). The EVE including electronic design tools (placement, routing, timing analysis, and synthesis programs) will automatically determine where in the IC design to insert additional flip-flops to maintain correct functionality of the IC design throughout the pipelining process (Sections 3-5). To evaluate EVE, Chow et al. teach that a full implementation of a set of baseline circuits from an automatic push-button flow is obtained (see section 5).

7. As to claims 6-7, 17-18 and 28-29, Chow et al. teach automatically determining where in the circuit to insert additional flip-flops to maintain correct functionality of the circuit throughout the pipelining process and to meet timing (See section 4). The selection of good physical placement for pipelining flip-flops minimizes the critical path delay .

8. As to claims 34-57, Chow et al. teach automatically where to insert additional flip-flops to maintain high functionality performance throughout the pipelining process using mixed programming electronic design tools to manually and automatically interactively

and iteratively perform the process of insertion of the flip-flops to meet parameters including operating frequency and an efficiency per cycle (See sections 3-5). It is noted that pipeline is used in a central processing unit (CPU).

9. As to claims 58-60, Chow et al. teach automatically where to insert additional flip-flops in the circuit to maintain high performance of circuit is done using electronic design tool (placement, routing, timing analysis and synthesis programs) (at least see sections 3 and 5).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2, 13 and 24 are rejected under 35 U.S.C. 103(a) as being obvious over Chow et al. "EVE: A CAD Tool for Manual Placement and Pipelining Assistance of FPGA Circuits," ACM, Feb. 2002, pp. 85-94 in view of Smits et al. (6,631,444).

12. As to claims 2, 13 and 24, although it is known to group signals into groups in pipelining and specifying rules, Chow et al. do not mention them. In order to resolve synchronization and timing problems along bus lines operating in pipelined fashion, Smits et al. teach inserting number of flip-flips, buffers or latches along the bus lines (rules for pipelining) or at specified one or more pipeline locations of the IC design (electronic design) (Fig. 4-5, col. 5 line 60 to col. 7 line 30). Smits et al. teach organizing

signals in the electronic design into groups (input data/address paths) (col. 6 lines 30-34; Fig. 4-5) and specifying rules for pipelining (col. 6, lines 1-9, number of inserted flip-flops, buffers or latches). It would have been obvious to practitioners in the art at the time the invention was made to organize signals in to groups and specifying rules for pipelining each signal group in order to resolve synchronization and timing program along bus lines operating in pipelined fashion.

Remarks

Examiner provides new grounds of rejection to clearly define that the claim limitations are not patentable. Applicants also request to consider van der Wal et al. (6,151,682) and Baldwin (6,798,421) regarding inserting of flip-flops in a pipeline and grouping signals and rules.

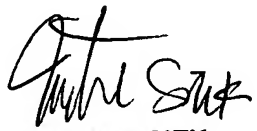
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER